Patent Assignment Abstract of Title

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Title: Data transfer and synchronization system

Assignment: 1

Reel/Frame: 010823/0356 **Received:** 06/06/2000 **Recorded:** 06/01/2000 **Mailed:** 07/29/2000 **Pages:** 3

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

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Search Results as of:

09/491,675

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	1911	(differen$4 same transmit$4 same transaction$1) and (network$4 or server$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 20:33
2	BRS	L2	21	L1 and (differenc$4 adj transmit$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 20:33
3	BRS	L3	383	((differen$4 same transmit$4 same transaction$1) and (network$4 or server$1)) and (differenc$4 same transaction$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 20:34
4	BRS	L4	31	L3 and (destination$1 or goal$1) and (data adj sourc$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 20:53
5	BRS	L5	2	5710922.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 20:53

	Document ID	Issue Date	Title	Current OR	Inventor
1	US 20030198251 A1	20031023	Fibre channel arbitrated loop bufferless switch circuitry to increase bandwidth without significant increase in cost	370/462	Black, Alistair D. et al.
2	US 20030174722 A1	20030918	Fibre channel arbitrated loop bufferless switch circuitry to increase bandwidth without significant increase in cost	370/403	Black, Alistair D. et al.
3	US 20030174721 A1	20030918	Fibre channel arbitrated loop bufferless switch circuitry to increase bandwidth without significant increase in cost	370/403	Black, Alistair D. et al.
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6	US 20030153273 A1	20030814	Vector network analyzer applique for adaptive communications in wireless networks	455/67.14	Ebert, Paul Michael et al.
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12	US 20030101307 A1	20030529	System of distributed microprocessor interfaces toward macro-cell based designs implemented as ASIC or FPGA bread boarding and relative common bus protocol	710/305	Gemelli, Riccardo et al.
13	US 20030055883 A1	20030320	Synthetic transaction monitor	709/203	Wiles, Philip V. JR.
14	US 20020087455 A1	20020704	Global foreign exchange system	705/37	Tsagarakis, Manolis et al.
15	US 20020087454 A1	20020704	Global trading system	705/37	Calo, Bea et al.
16	US 20020040369 A1	20020404	Binary data synchronization engine	707/201	Multer, David L. et al.

	Document ID	Issue Date	Title	Current OR	Inventor
17	US 20020029227 A1	20020307	Management server for synchronization system	707/203	Multer, David L. et al.
18	US 20020015042 A1	20020207	Visual content browsing using rasterized representations	345/581	Robotham, John S. et al.
19	US 20020010807 A1	20020124	Data package including synchronization data	709/328	Multer, David L. et al.
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21	US 20010044805 A1	20011122	Synchronization system application object interface	707/201	Multer, David L. et al.
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23	US 6614796 B1	20030902	Fibre channel arbitrated loop bufferless switch circuitry to increase bandwidth without significant increase in cost	370/403	Black, Alistair D. et al.
24	US 6606744 B1	20030812	Providing collaborative installation management in a network-based supply chain environment	717/174	Mikurak, Michael G.
25	US 6601037 B1	20030729	System and method of processing credit card, e-commerce, and e-business transactions without the merchant incurring transaction processing fees or charges worldwide	705/14	Kolls, H. Brock
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27	US 6473794 B1	20021029	System for establishing plan to test components of web based framework by displaying pictorial representation and conveying indicia coded components of existing network framework	709/223	Guheen, Michael F. et al.
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31	US 4837786 A	19890606	Technique for mitigating rain fading in a satellite communications system using quadrature phase shift keying	370/206	Gurantz, Itzhak et al.